2. (Once amended) A method of interfacing frame based TDM telecommunications traffic in which each TDM frame supports a plurality of data structures each comprising one or more channels from a frame-based TDM network to an asynchronous network in which traffic is transported in cells or packets, the method comprising;

issuing credits at a substantially constant rate;

assigning the credits to each said data structures according to the size of that data structure;

determining for each said data structure a threshold number of assigned credits; and,

when said threshold value is reached, assembling that data structure into cells or packets for despatch into the asynchronous network.

4. (Once amended) A method as claimed in claim 3, wherein said connection control assigns credits to a data structure by writing the identity of that data structure into free locations in a reverse channel map.

9. (Once amended) An interface arrangement for interfacing frame based TDM telecommunications traffic from a frame-based TDM network to an asynchronous network, the arrangement being arranged to map the frame-based TDM traffic into cells, and incorporating a scheduler for scheduling the despatch of said cells into the asynchronous network at a substantially constant rate.

10. (Once amended) An interface arrangement for interfacing frame based TDM telecommunications traffic in which each TDM frame supports a plurality of data structures each comprising one or more channels from a frame-based TDM network to an asynchronous network in which traffic is transported in cells or packets, the method comprising;

means for issuing credits at a substantially constant rate;

means for assigning the credits to each said data structures according to the size of that data structure; and

means for determining for each said data structure a threshold number of assigned credits whereby, when said threshold value is reached, the data structure is assembled into cells or packets for despatch into the asynchronous network.

17. (Once amended) A method of scheduling despatch of a TDM data structure packetized into cells or packets for despatch into an asynchronous network, the method comprising allocating credits to the data structure at a predetermined rate, comparing the accumulated total of credits for said data structure, and, when said total reaches a predetermined threshold, despatching said cells into the asynchronous network at a substantially constant rate.

In the Specification

Please amend the specification as follows:

Page 6, lines 17 – 30:

A Frame Clock 51 is used to provide the synchronous timing mechanism required to control the scheduler process. Typically the clock is used to provide two levels of timing control, the frame signal and the intra-frame timing signal, here referred to as a tick. The frame signal as its name implies is used to provide a periodic framing signal. For example, in the case of PCM voice this framing signal would be generated once every 125 µs corresponding to the frame rate. The intra-frame timing signal or tick is used to provide timing within the frame, the resolution of the tick being at least equal to the number of synchronous data channels supported by the device. For example a scheduler designed to schedule the assembly of 8000 synchronous data channels into a number of data packet structures would require at least 8000 ticks per frame. In reality the number of ticks may be set to slightly larger than the number of synchronous data channels, the additional 'ticks' providing tolerance or slack within the basic scheduling algorithm to enable housekeeping and other control tasks to be interleaved within the basic scheduling algorithm.

Page 7, lines 5 – 33:

The rate of generation of credits and the intervals within the frame period at which each credit is issued is determined by a reverse channel map 23. The reverse channel map contains one location of memory per synchronous data channel supported by the scheduler device. Thus in the 8000 channel example the table would contain 8000 channels. Each location of the map contains the identity of the data structure to be credited. The scheduler creditor process 52 reads the map in a cyclic manner driven by the frame clock ticks so that each location of the map is read exactly once per frame.

A connection control process 2 is used to configure and control the reverse channel map 23. At scheduler initialization, all locations within the map 23 are set to null to indicate that there is nothing at present to schedule. To begin scheduling the assembly of a data structure the connection control process 2 assigns credits to that data structure by writing its identity into free locations in the map 23. The number of locations, i.e. credits, assigned to the data structure is directly proportional to its data rate. The locations that are assigned to the data structure dictate, within the frame interval the timing distribution for the assembly of its credits. Therefore the algorithm that the connection control process uses to assign free locations to a data structure will dictate the scheduling distribution for that structure. The scheduler process described will support any chosen algorithm for this process. The appropriate algorithm may thus be selected to suit the desired timing solutions for a particular application. Potential options for the allocation of free slots include but are not limited to the following.

The connection control process 2 uses a substantially random process to allocate free slots to the data structures. Particularly for large data structures where the number of data channels is greater than the nominal packet size, this will tend to ensure overall a random scheduling of packets within the frame interval and thus provides an effective mechanism to limit jitter.